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ECG 722: Mixed-Signal Circuit Design

K-Delta-1-Sigma Modulator

Introduction

The KD1S Modulator is a high-resolution ADC that incorporates the delta-sigma topology with the capability of adjusting the "delta" to a K number of adjustable feedback quantizing paths with 1 "sigma" from the use of 1 integrator. This topology was proposed due to the need for higher speeds in transistors as we scale down their sizing, but due to the higher speeds required, designs are now limited to lower gain, increased leakage current, prone to more mismatches. The KD1S modulators discussed and designed in this paper are the 8-Path first order and 4-path second order modulators within a continuous time topology.

Design

The KD1S modulator designed in this paper makes use of a voltage-controlled oscillator, self-biased differential amplifiers, comparators, transmission gates, and an 8-bit register.

Clock Generator:

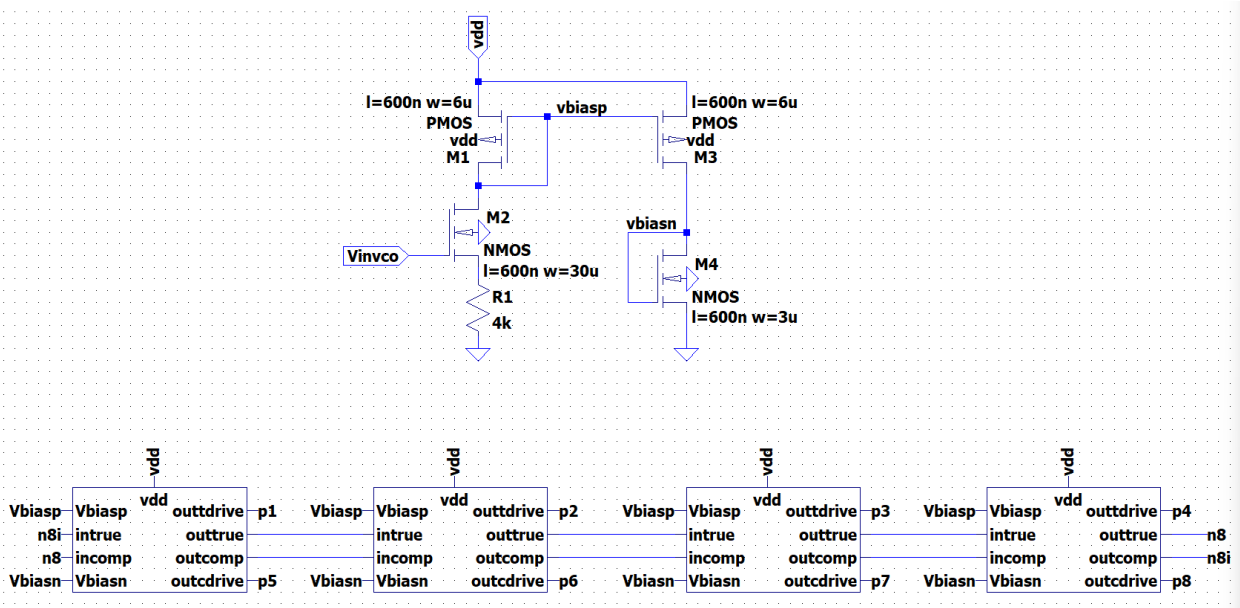


Figure 1. Top: Linear Voltage Controller. Bottom: Delay blocks

The clock generator used in this topology is seen above. Since we are using an 8-path topology for our first order KD1S, we can use the 4 delay blocks seen below in this configuration to generate 8 clock cycles that are equally out of phase. Above the delay blocks is a linear voltage-controlled CMOS circuit topology used to control the frequency of our oscillator used to adjust our sampling frequency. Below is the circuit schematic for the delay blocks used for this oscillator.

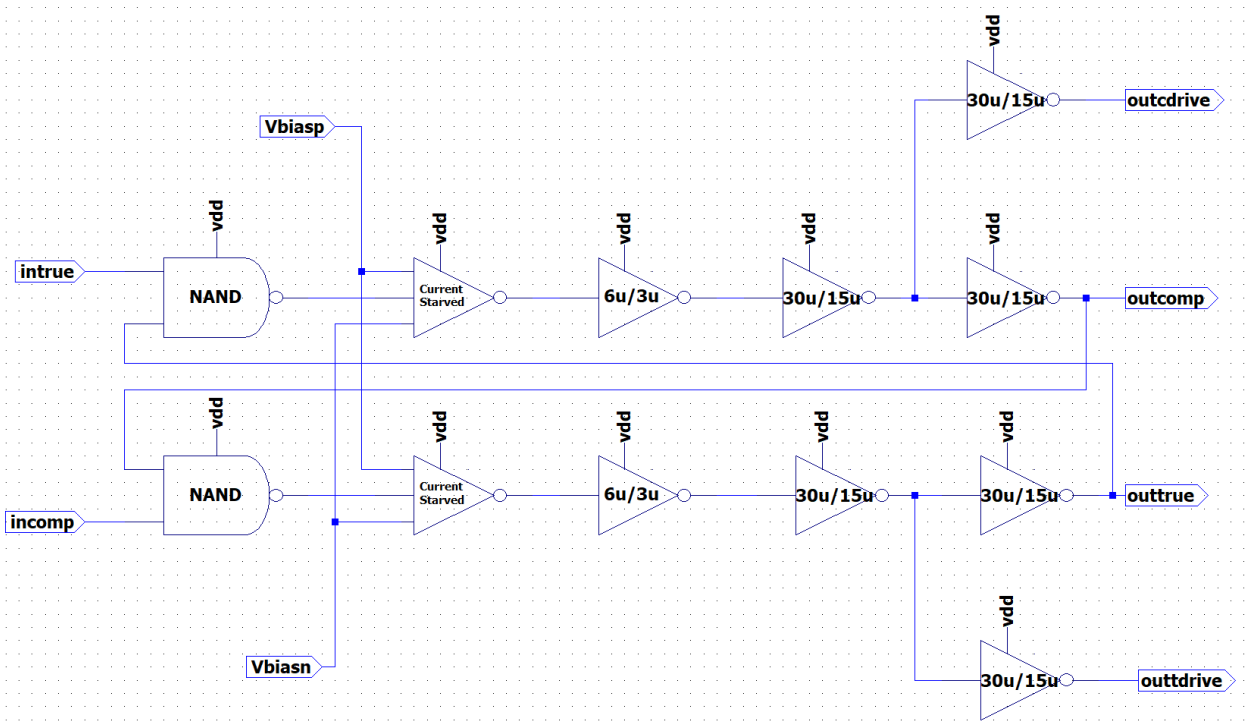


Figure 2. SR Latch configuration inside the delay block

The delay block incorporates NAND gates, current starved inverters, and regular inverters with different sizing in an SR latch configuration to give complementary outputs. The current starved inverters control how much current flows through the circuit and is adjusted through the Vbiasp and Vbiasn inputs. These two inputs are connected to the linear voltage controller and is adjusted through the VinVCO input, which is how the frequency is adjusted for our overall sampling frequency. This is a convenient method of adjusting the frequency through one input voltage adjustment.

Clock Generator Simulation:

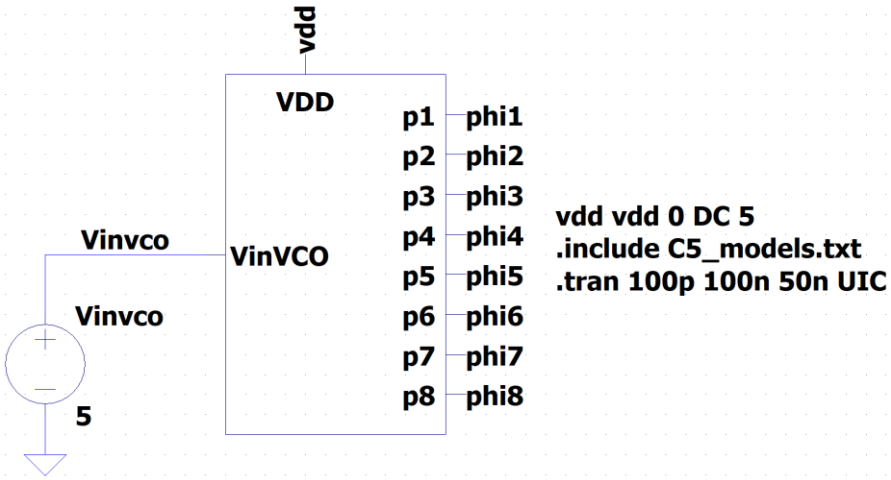


Figure 3. Symbol used for the VCO

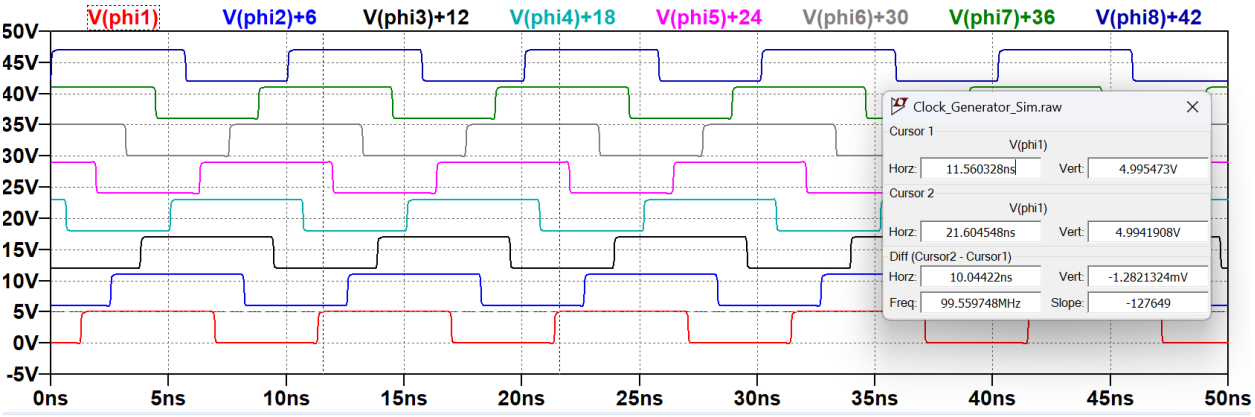


Figure 4. Simulation results for the clock signals

We can see from the simulation above that our VCO outputs about 100MHz given that our VinVCO source is at 5V. What's important to note is that each clock output is non-overlapping, with each phi adding about a 1.25ns delay going from phi1 – phi8 (since we need a K number of cycles for a K number of paths. We also note that our duty cycle is not 50%, but a little more since we see that our clock is high a little bit more than it is low. This does not affect our performance since we are mainly looking for sharper rise times (sharper edges and more square waves) and this is shown to be successful through how we wired up our SR latch circuit.

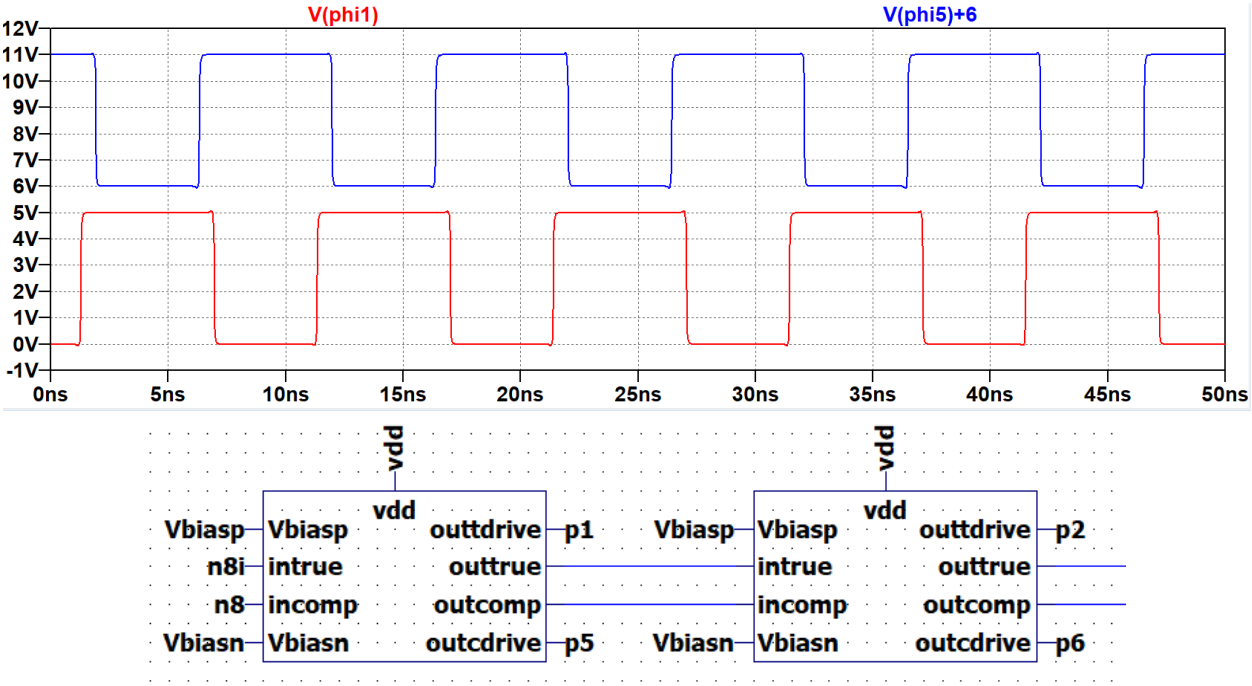


Figure 5. Example of a clock signal and its complement

In the figure above, we see that we achieve sharp rise times through our clock generator. We can also note that phi1 and phi5 are about 180 degrees out of phase, but not quite perfectly out of phase. This is due to the delay configuration and what we labelled as coming out of each delay block, seen below. Since the output of each delay block is its complementary signal, we can see that phi1 and phi5 are complements, along with phi2 and phi6, phi3 and phi7, and phi4 and phi8.

How out of phase they are would depend on what lengths and widths we chose for our inverters and how strong we drive them within the delay block/SR latch configuration.

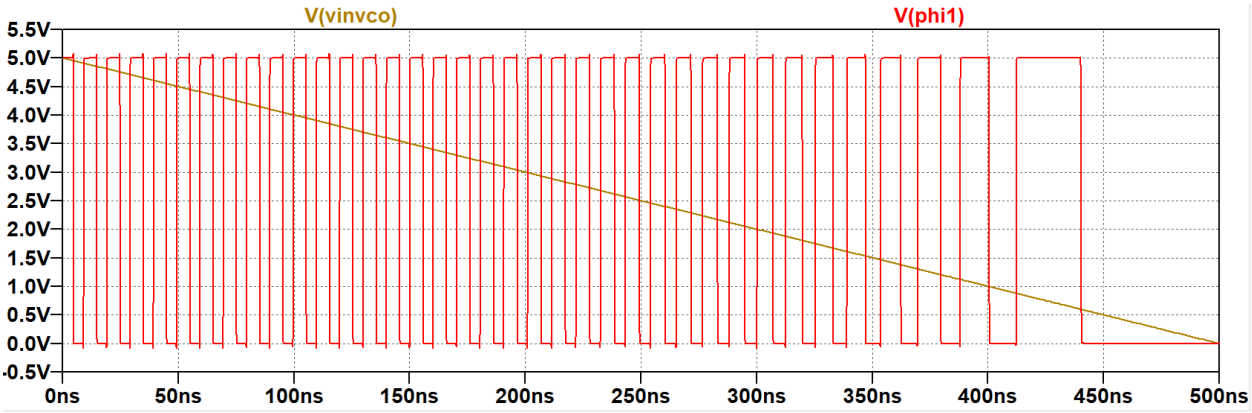


Figure 6. Ramp simulation of VinVCO with relation to a clock signal

This figure shows that with a linear ramp going from 5V to 0V fed into our VinVCO, we can see that adjusting our VinVCO changes our oscillating frequency. We can note that our VinVCO does not work below 0.7V, which is the threshold voltage of the NMOS within the linear voltage controller. The resistor connected in the linear voltage controller adjusts how much current flows through this controller, thus linearly adjusting the maximum frequency the whole clock generator switches at. We set this resistor to 4k, giving us 100MHz at 5V as our maximum VinVCO input and frequency.

At the maximum VinVCO, our current starved inverters have a shorter delay since more current flows through the transistors as our gate is “opened” to its fullest, thus overall increasing our switching frequency through the delay blocks. These changes in frequencies is noted in the table below at different VinVCO voltages.

VinVCO	Frequency
5V	~100MHz
4V	~100MHz
3V	~97MHz
2V	~83MHz
1V	~41MHz
0.7V	~16MHz

Amplifier:

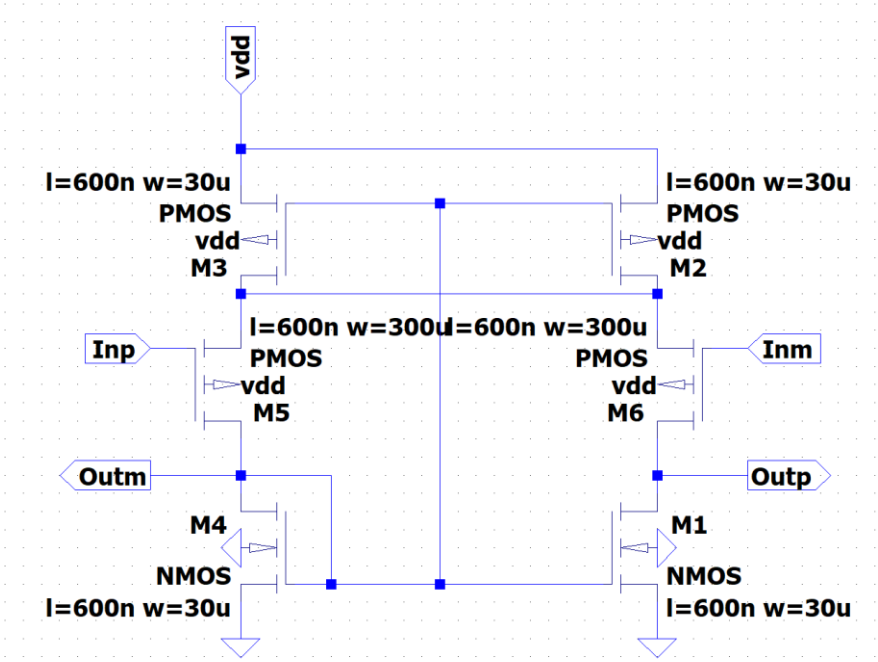


Figure 7. Differential amplifier circuit

The amplifier used in this design is the one seen above, which is a self-biased amplifier. This topology is used since it is simple, consumes low power, has enough gain for our use, and has no slew rate limitations (high speed). Below we see the symbol used in our overall topology and is connected as the modulator's integrator.

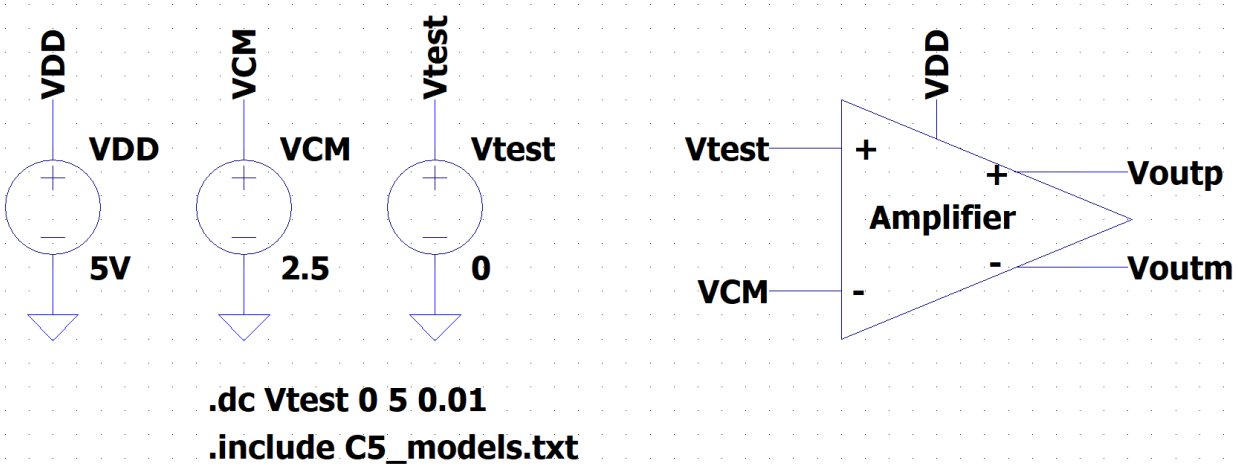


Figure 8. Symbol used for the amplifier

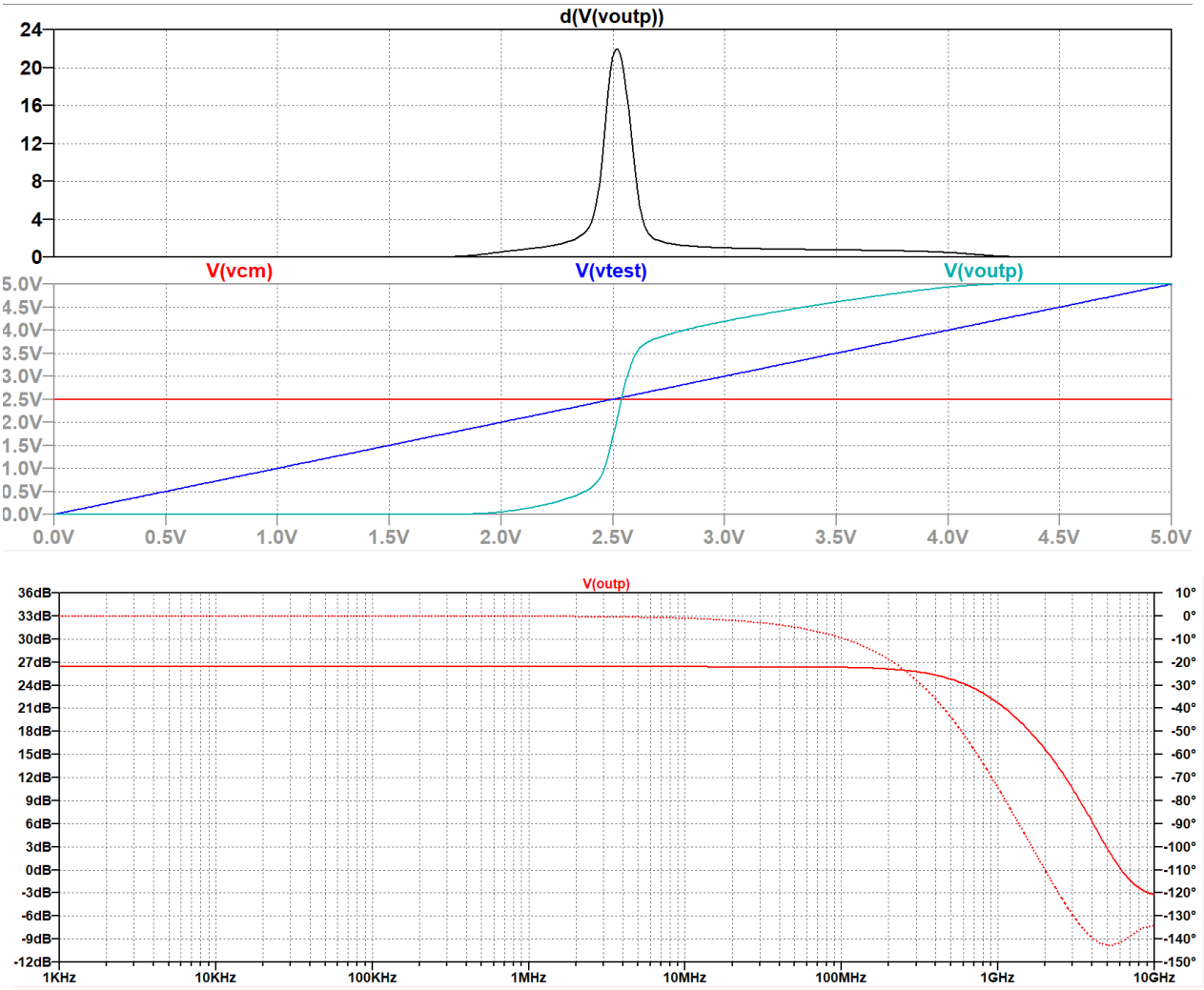


Figure 9. Simulation results for the amplifiers gain (top) and bode plot (bottom)

The above simulation shows that this amplifier gives us a gain of about 22, which is sufficient for our 8-Path and 4-path topologies, as well as the bode plot of the open-loop gain which shows that our amplifier should give a consistent gain up to 100-200MHz, which is sufficient for the limits of this design.

Note that we need cannot have a frequency that is too low within our integrator, otherwise we will reach integration saturation, so we need to be switching at a reasonably fast rate, and we can adjust this by changing our resistor and capacitor values to prevent saturation, which was done during the simulation phase of this project (shown later in the report).

Comparator:

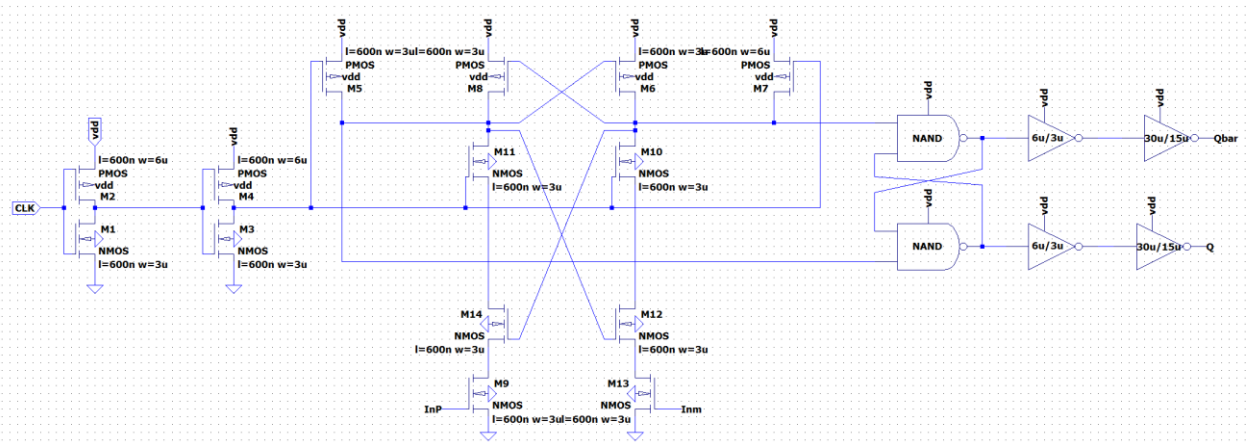


Figure 10. Comparator circuit

The comparator used in the KD1S modulator is seen in the figure above. To the left of the comparator are two inverters to drive the signal's input stronger. To the right of the comparator is the SR latch used to make sure that the outputs are never on at the same time (to prevent them from overlapping) and produce a complementary signal (Q and Qbar). This comparator's benefits are that it has no memory since there are no dynamic nodes assuming that the inputs are above the threshold voltage, otherwise the amplifier will fail to turn on since M9 and M13 will not turn on and provide a proper path to ground for the circuit to sense properly. Having no memory allows this comparator to make accurate decisions at high speeds. This comparator also has reduced kickback noise since the inputs are isolated from the latch by M9 and M13. Below is the simulation test to determine how well the comparator makes a decision, as well as the symbol used for the comparator in our KD1S design.

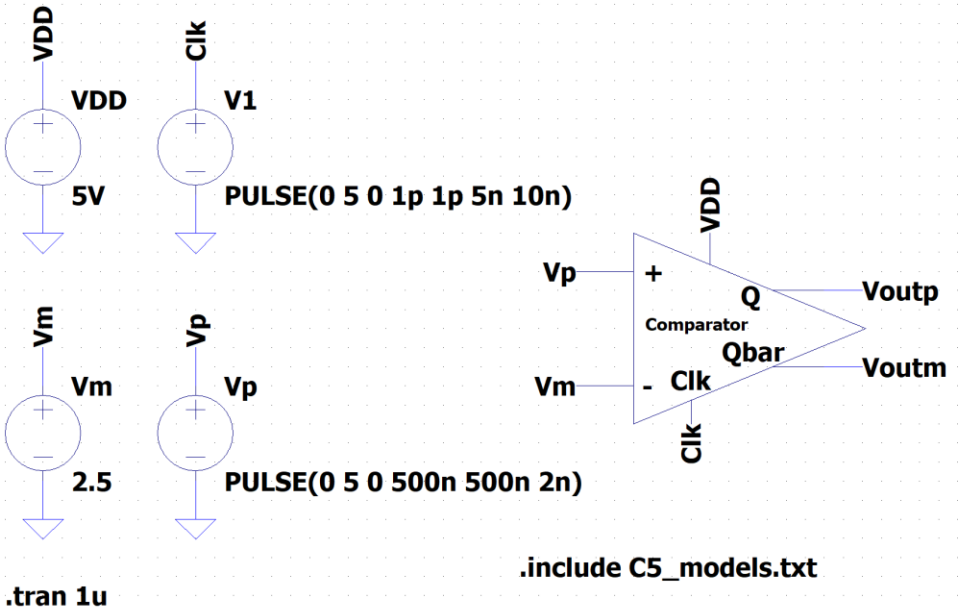


Figure 11. Symbol for the comparator used

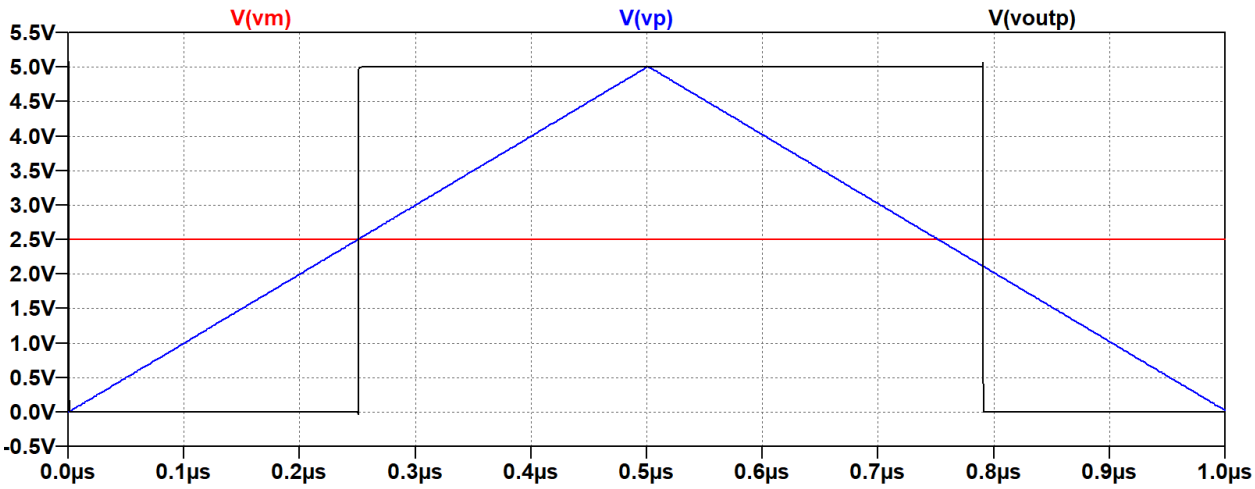


Figure 12. Simulation results for the comparator

We can see from the test above that our comparator can make a decision almost instantly and has a fairly quick decision-making ability for an input's rising edge, which we care more than our falling edge in our overall modulator.

Feedback Signal Control and Logic:

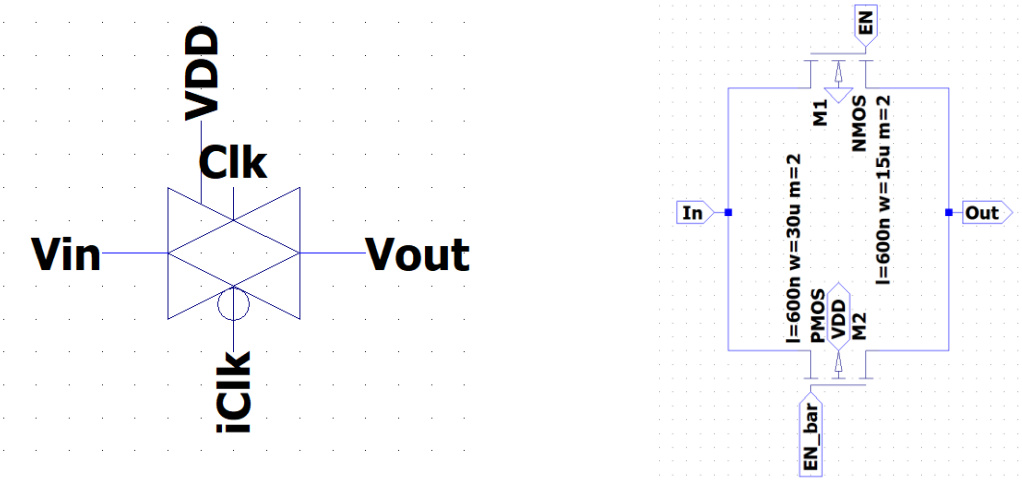


Figure 13. Transmission gate symbol and circuit

For our feedback control, instead of using switched capacitors, we will be using transmission gates (TG's) to be placed in the feedback path of our KD1S modulator. The transmission gate acts as a CMOS switch which allows a signal to either pass through or prevent it from passing. How this operates is through the PMOS and NMOS gates, where the clock inputs are complementary from each other. When the clock passes a high, the NMOS turns on, and simultaneously the inverted clock passes a low to the PMOS which also turns it on, fully allowing our signal to pass. Similarly, this works the same way for when the NMOS is fed a low clock (PMOS is fed a high), keeping the TG off, preventing any signal from passing. The benefit of a transmission gate is that it allows full logic levels to pass through without the voltage drop of the threshold voltage of any transistors. This topology also allows clear signals to pass through without any leakage and low resistance.

8 Path 1st Order KD1S Modulator:

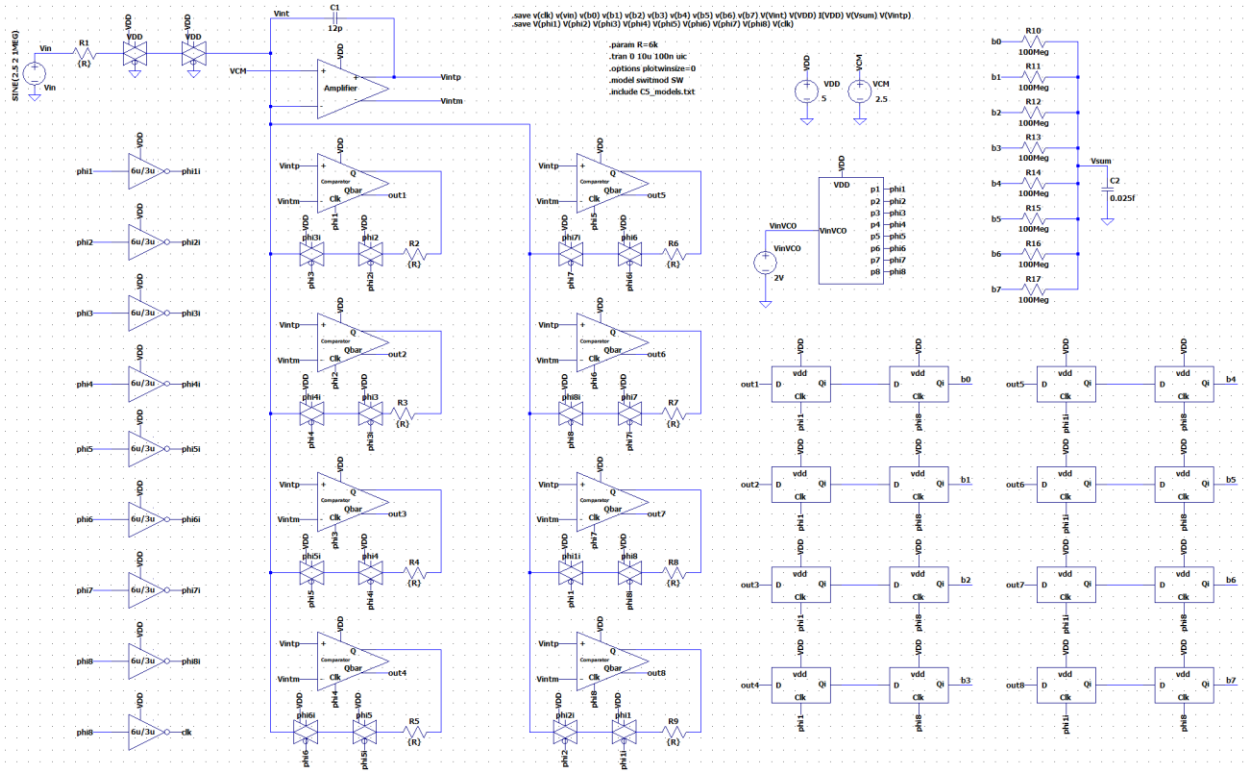


Figure 14. 8 Path 1st Order KD1S Modulator Design

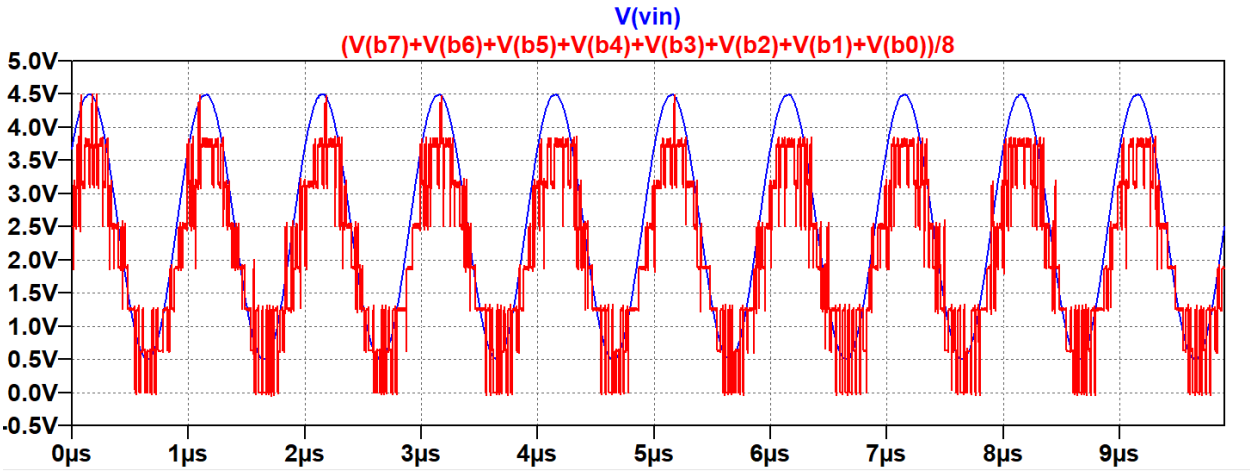
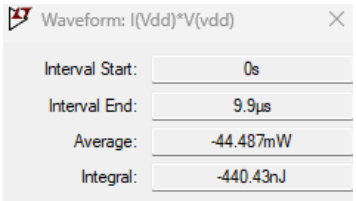


Figure 15. Simulation waveform running at an input frequency of 1MHz

Power Consumption (First Order, 8 Path):



Ideal SNR Hand Calculations:

$$SNR_{Ideal} = 6.02N + 1.76 - 5.17 + 30logK$$

$$where, \qquad K = K_{path} \cdot K_{avg} = OSR = 64, \qquad N = 1$$

$$SNR_{Ideal} = 6.02 + 1.76 - 5.17 + 30\log(64)$$

$$SNR_{Ideal} = 56.8\ dB$$

Effective number of bits:

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{42.8 - 1.76}{6.02} = 9.14\ bits$$

This is our ideal SNR for **OSR = 64**, similarly:

OSR = 128

$$SNR_{Ideal} = 6.02 + 1.76 - 5.17 + 30\log(128)$$

$$SNR_{Ideal} = 65.8\ dB$$

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{65.8 - 1.76}{6.02} = 10.6\ bits$$

OSR = 256

$$SNR_{Ideal} = 6.02 + 1.76 - 5.17 + 30\log(256)$$

$$SNR_{Ideal} = 74.9\ dB$$

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{74.9 - 1.76}{6.02} = 12.1\ bits$$

Overall Performance:

Input Frequency = 1MHz						
OSR	**64**		**128**		**256**	
Mode	**Serial**	**Parallel**	**Serial**	**Parallel**	**Serial**	**Parallel**
Fs new(MHz)	663	83	663	83	663	83
SNR (dB)	36.81	25.22	40.27	33.99	44.99	41.11
Neff (bits)	5.82	3.89	6.39	5.35	7.18	6.53
Bandwidth (MHz)	5.18		2.59		1.29	
Power Consumption	44.5mW					

Comparison with Fig. 9.32:

Input Frequency = 1MHz						
OSR	**64**		**128**		**256**	
Mode	**Serial**	**Parallel**	**Serial**	**Parallel**	**Serial**	**Parallel**
Fs new (MHz)	1830	228	1830	228	1830	228
SNR (dB)	39.82	36.16	45.68	41.72	59.51	60.02
Neff (bits)	6.32	5.71	7.29	6.63	9.59	9.67
Bandwidth (MHz)	14.29		7.15		3.57	
Power Consumption	68.55mW					

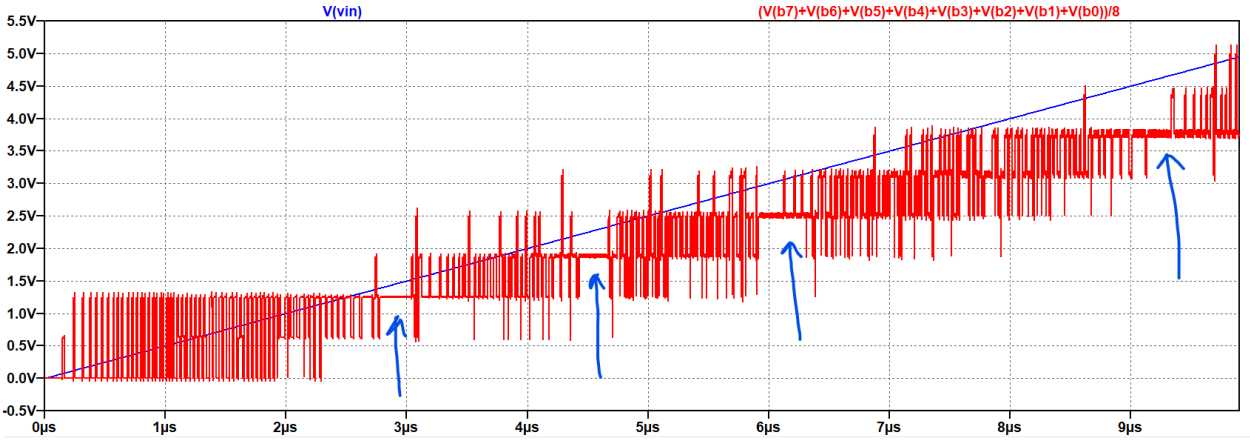


Figure 16. Ramp input to identify the dead zones (labelled in blue arrows)

We can see from the tables and simulation waveforms that our 8-Path 1st Order KD1S topology works as expected, with reasonably good SNR values shown in the table above when compared to the ideal values that were hand calculated. They are not exactly accurate due to external effects from the nonideal components used. We can see from Fig. 16 that when using a ramp input, we can spot the dead zones that were present within this topology. Comparing our SNR values from the ones in Fig. 9.32, we can also note that we get similar SNR values, but with the main difference in our parameters being that the sampling frequency in Fig. 9.32 is different than the one used in this design (83MHz compared to 228MHz). However, the power consumption with the design used in this paper was much lower than the one in Fig. 9.32 (44.5mW compared to 68.55mW). This lower power consumption is likely to have caused the lower SNR values too as a tradeoff in the design.

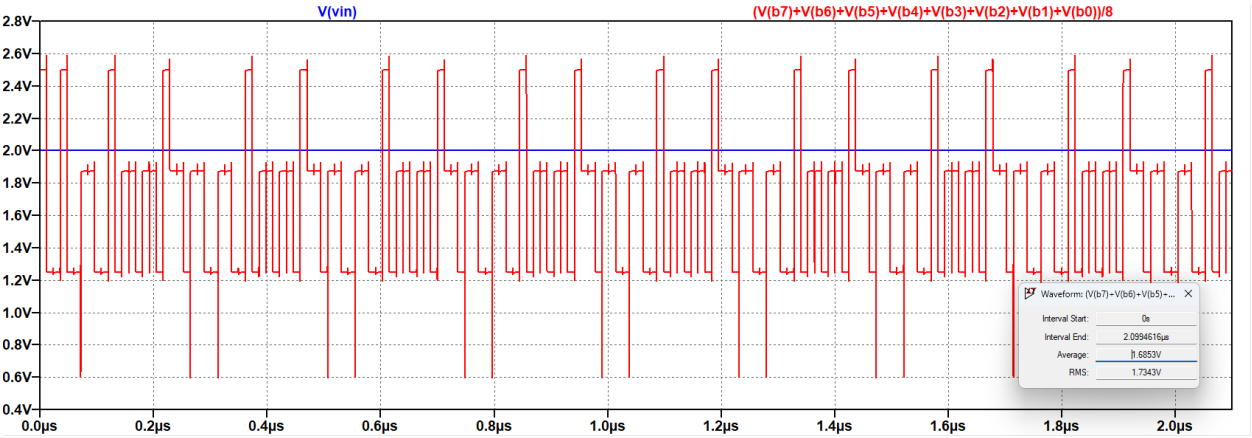


Figure 17. DC input for our 8 Path 1st Order KD1S

MATLAB Simulations:

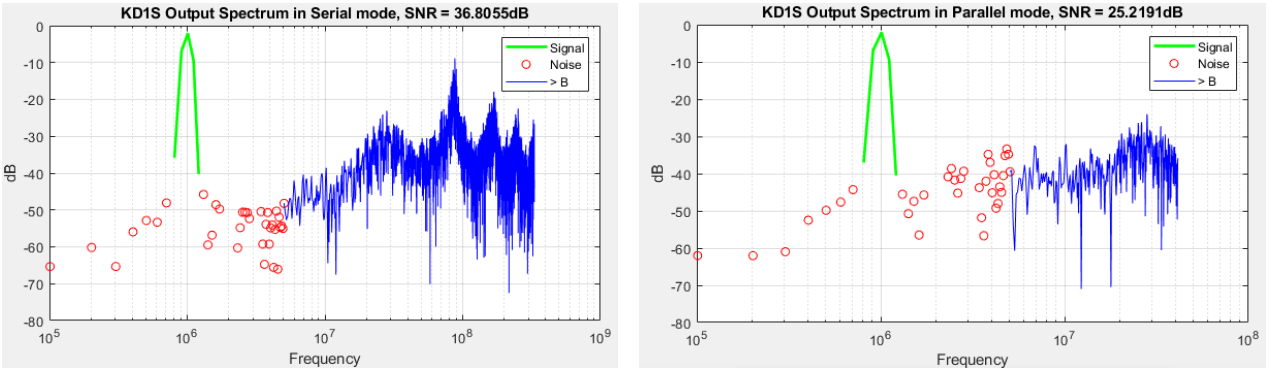


Figure 18. Output Spectrum for 8 Path 1st Order KD1S at OSR = 64

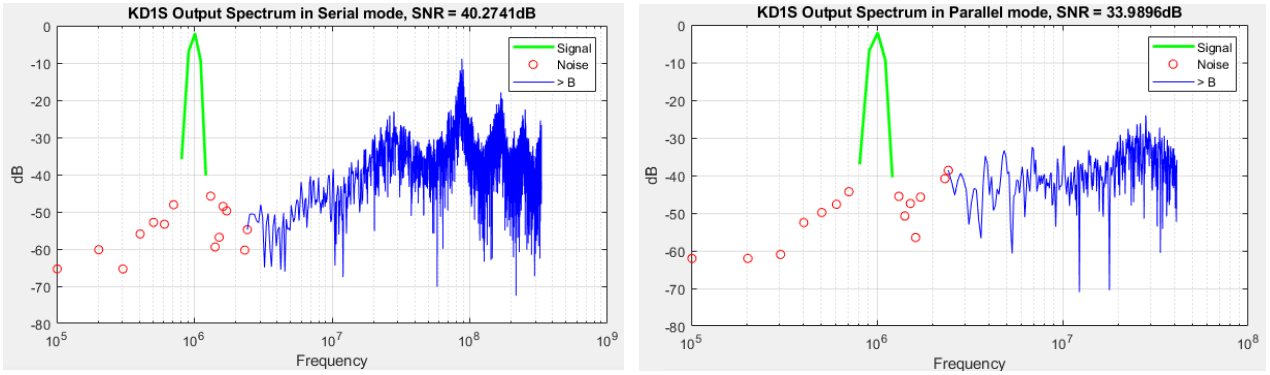


Figure 19. Output Spectrum for 8 Path 1st Order KD1S at OSR = 128

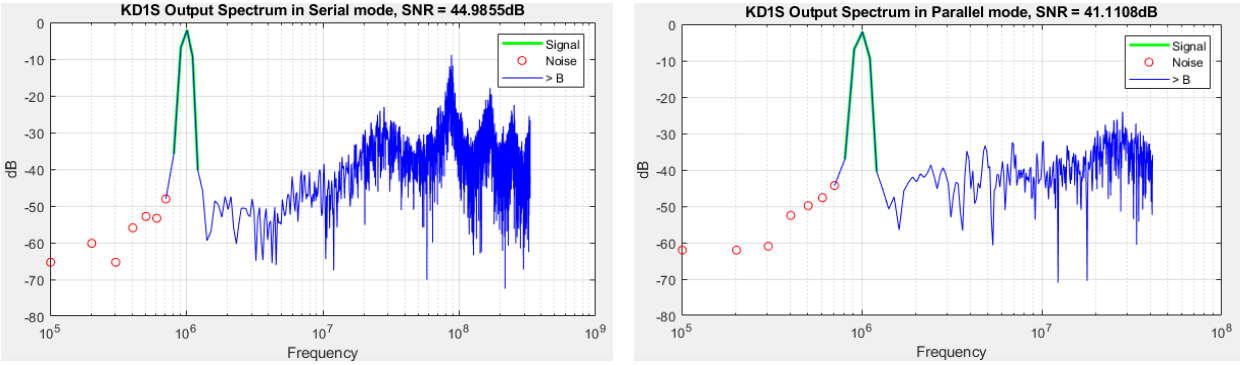


Figure 20. Output Spectrum for 8 Path 1st Order KD1S at OSR = 256

Fig. 17 shows that our design also works with a DC input, with our input being 2V and our design outputting an average of 1.68V, which is about 200mV off and seems reasonable. The MATLAB outputs are also shown for different OSR values shown in Fig. 18-20 to produce the spectrums of our signal and noise.

In the table below, different values were also tested for this design to see which produced the best SNR results. The best results came at the input frequency that was finalized upon (1MHz) along with a sampling frequency of 83MHz. The results of the trials at different input frequencies, sampling frequencies, and amplitudes are shown below:

Input frequency	Amplitude	C	R	VCO/Sampling f	OSR	SNR (S)	SNR (P)	Neff (S)	Neff (P)	Band MHz
1MHz	2	12pF	6k	2V/83MHz	64	36.81	25.22	5.82	3.89	5.18
1MHz	2	12pF	6k	2V/83MHz	128	40.27	33.99	6.39	5.35	2.59
2MHz	2	12pF	6k	2V/83MHz	64	33.55	26.57	5.28	4.12	5.17
2MHz	2	12pF	6k	2V/83MHz	128	36.56	32.44	5.78	5.09	2.59
3MHz	2	12pF	6k	2V/83MHz	64	32.84	27.47	5.16	4.27	5.18
3MHz	2	12pF	6k	2V/83MHz	128	38.63	32.13	6.12	5.04	2.59
1MHz	2	12pF	6k	1.8V/77MHz	64	35.41	26.37	5.59	4.09	4.85
1MHz	2	12pF	6k	1.8V/77MHz	128	40.47	36.37	6.43	5.75	2.42
1MHz	1.8	12pF	6k	1.8V/77MHz	64	34.45	26.40	5.43	4.09	4.85
1MHz	1.8	12pF	6k	1.8V/77MHz	128	39.82	37.00	6.32	5.85	2.42
1MHz	2	12pF	6k	5V/100MHz	64	27.31	25.73	4.24	3.98	6.27
1MHz	2	12pF	6k	5V/100MHz	128	31.49	30.79	4.93	4.82	3.13

We can note that increasing our input frequency doesn't affect the SNR that much, neither does changing the amplitude by small amounts. However, what we set our VinVCO voltage to (to adjust the sampling frequency) seems to affect the design the most, with lower sampling frequencies being more optimal in this design since our SNR seems to be higher at 77MHz than it does at 100MHz for example, with an SNR difference of about 10dB in serial mode. Parallel mode SNR doesn't get affected by this change in sampling frequency, which is to be expected since the serial sampling frequency would be the product of the K number of paths with the sampling frequency (8*83MHz in this case to give a new frequency of 664MHz.

4 Path 2nd Order KD1S Modulator:

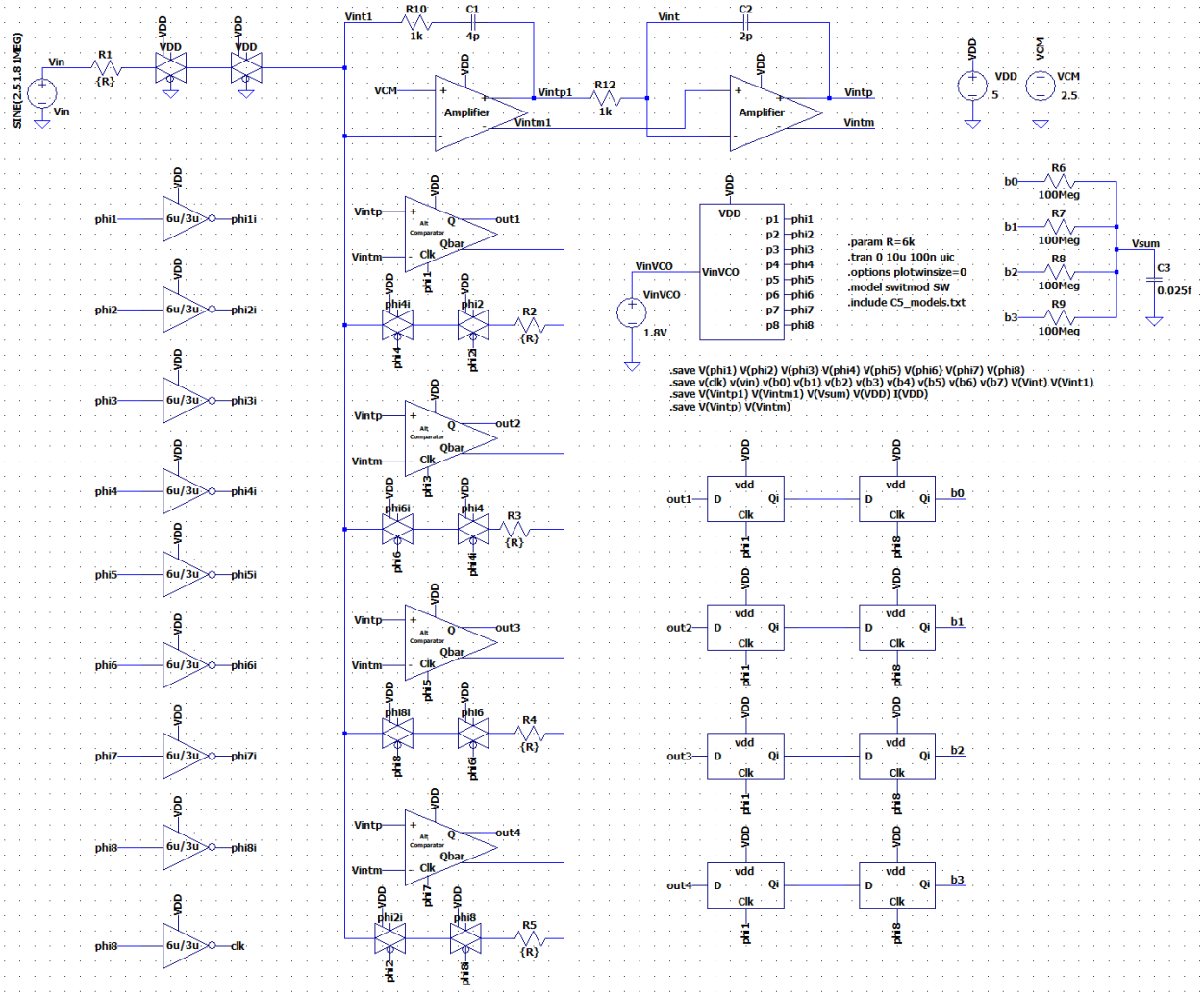


Figure 21. 4 Path 2nd Order KD1S Modulator Design

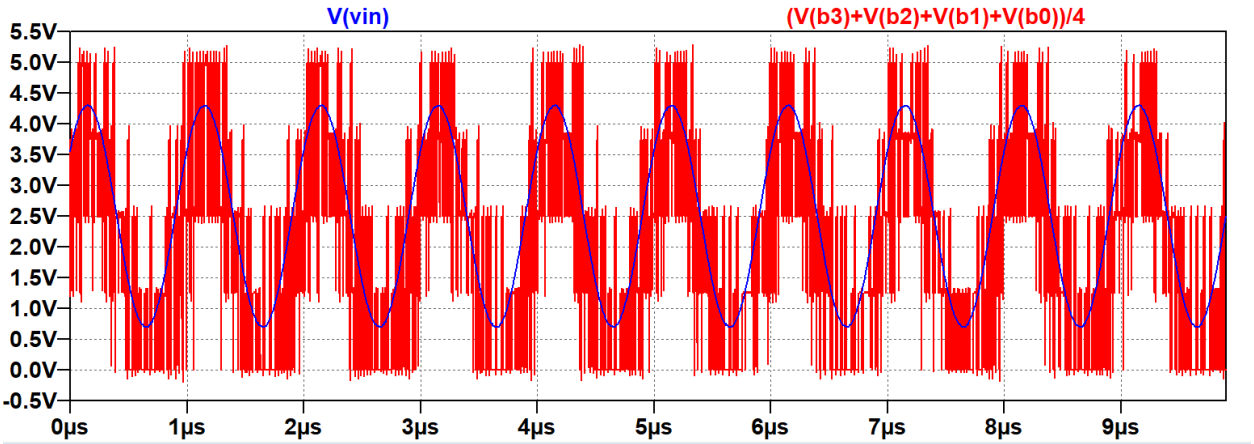


Figure 22. Simulation waveform running at an input frequency of 1MHz

Ideal SNR Hand Calculations:

$$SNR_{Ideal} = 6.02N + 1.76 - 12.9 + 50logK$$

$$where, \qquad K = K_{path} \cdot K_{avg} = OSR = 32, \qquad N = 1$$

$$SNR_{Ideal} = 6.02 + 1.76 - 12.9 + 50\log(32)$$

$$SNR_{Ideal} = 70.1\ dB$$

Effective number of bits:

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{47.8 - 1.76}{6.02} = 11.4\ bits$$

This is our ideal SNR for **OSR = 32**, similarly:

OSR = 64

$$SNR_{Ideal} = 6.02 + 1.76 - 12.9 + 50\log(64)$$

$$SNR_{Ideal} = 85.2\ dB$$

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{85.2 - 1.76}{6.02} = 13.9\ bits$$

OSR = 128

$$SNR_{Ideal} = 6.02 + 1.76 - 12.9 + 50\log(128)$$

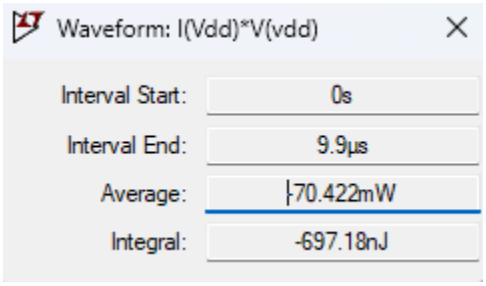
$$SNR_{Ideal} = 100\ dB$$

$$N_{eff} = \frac{SNR_{Ideal} - 1.76}{6.02} = \frac{100 - 1.76}{6.02} = 16.3\ bits$$

Overall Performance:

Input Frequency = 1MHz						
OSR	**32**		**64**		**128**	
Mode	**Serial**	**Parallel**	**Serial**	**Parallel**	**Serial**	**Parallel**
Fs new(MHz)	331	83	331	83	331	83
SNR (dB)	39.40	34.41	42.55	40.92	45.69	45.44
Neff (bits)	6.25	5.42	6.77	6.50	7.29	7.25
Bandwidth (MHz)	5.17		2.58		1.29	
Power Consumption	70.4mW					

Power Consumption (Second Order, 4 Path):



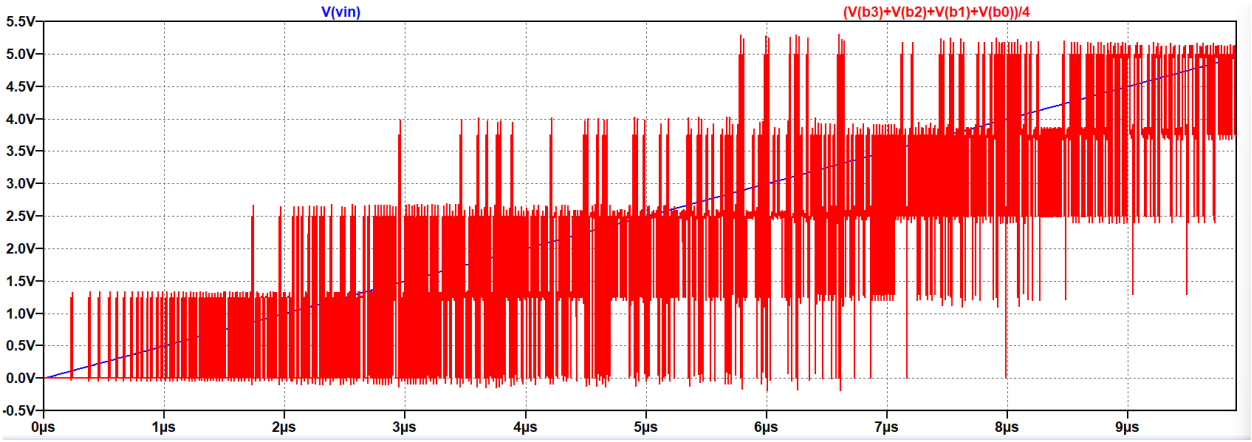


Figure 23. Ramp input to identify the dead zones

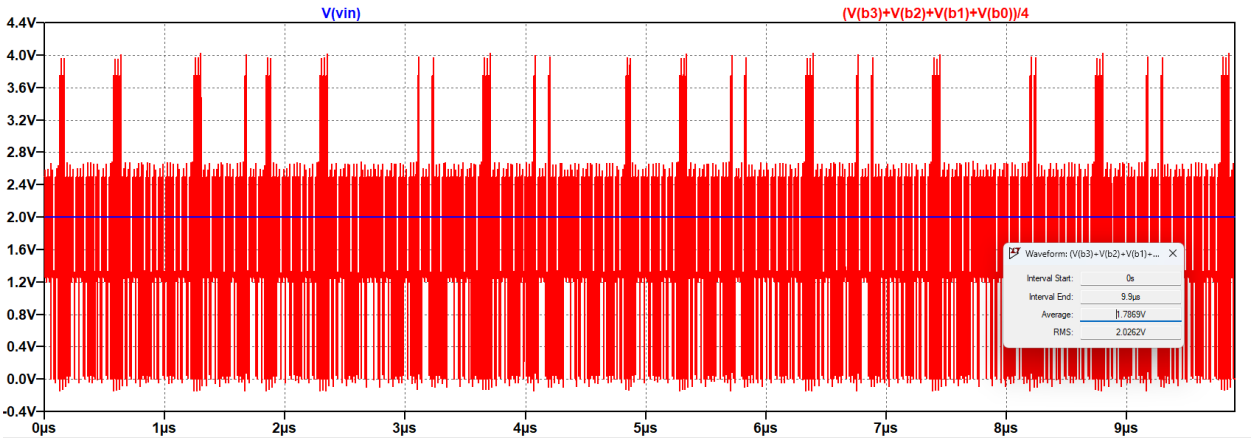


Figure 24. DC input for our 4 Path 2nd Order KD1S

The figures above showed similar methods of testing the second order topology as was done in the first order. We can notice that for the same bandwidth and sampling frequency as the first order, the second order performed better than the first order in a few ways. For one, we see better SNR results than the first order version, but it did come at the cost of producing more power (44.5mW for the first order compared to the 70mW second order). This is expected since we have an extra integrator which would use up more power. With this SNR advantage, we can also note that the first order topology was more prone to dead zones that were more explicitly seen within a 10us time window, making the second order topology better once more. Finally, applying a DC input showed that we can average an output of about 1.78V, which is 100mV better than the previous result of 1.68V for the first order. These improvements make the second order topology better in many ways, at the slight cost of more power being used.

MATLAB Simulations:

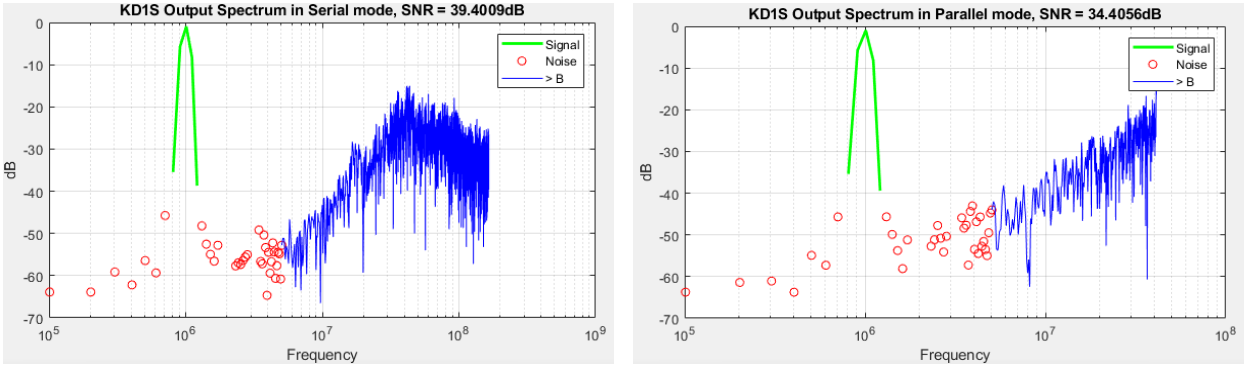


Figure 25. Output Spectrum for 4 Path 2nd Order KD1S at OSR = 32

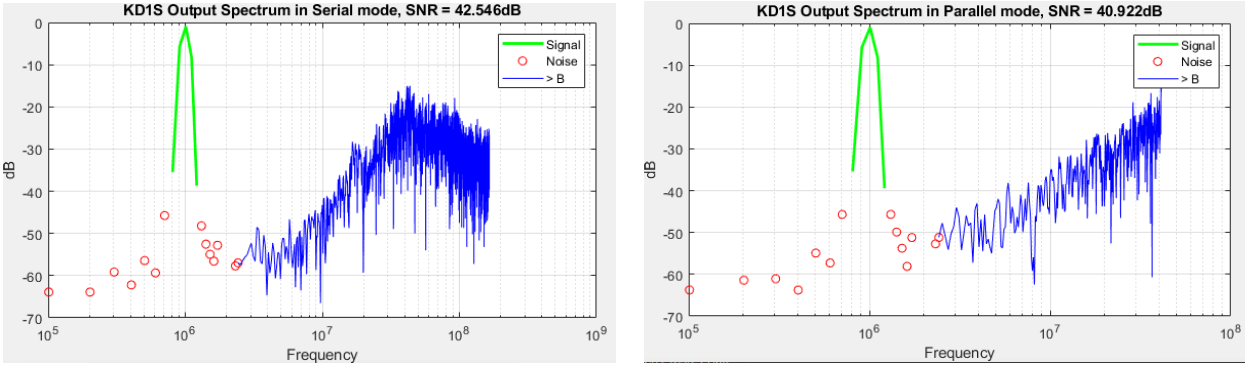


Figure 26. Output Spectrum for 4 Path 2nd Order KD1S at OSR = 64

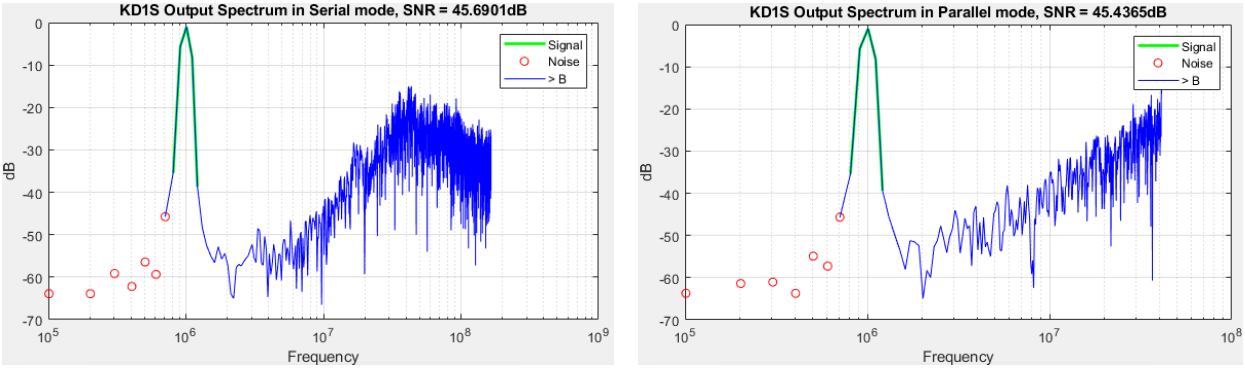


Figure 27. Output Spectrum for 4 Path 2nd Order KD1S at OSR = 128

Trials at different input frequencies, sampling frequencies, and amplitudes for the 4-Path 2nd Order KD1S modulator:

Input freq.	Amp	C1	C2	R	VCO/Sampling freq	OSR	SNR (S)	SNR (P)	Neff (S)	Neff (P)	Band MHz
1MHz	1.8	4pF	2pF	6k	1.8V/77MHz	32	39.18	33.67	6.21	5.30	4.85
1MHz	1.8	4pF	2pF	6k	1.8V/77MHz	64	44.24	41.31	7.05	6.57	2.42
2MHz	1.8	4pF	2pF	6k	1.8V/77MHz	32	37.41	31.64	5.92	4.96	4.85
2MHz	1.8	4pF	2pF	6k	1.8V/77MHz	64	40.16	40.37	6.38	6.41	2.42
3MHz	1.8	4pF	2pF	6k	1.8V/77MHz	32	34.31	31.75	5.40	4.98	4.85
3MHz	1.8	4pF	2pF	6k	1.8V/77MHz	64	47.06	41.42	7.52	6.58	2.42
1MHz	1.8	4pF	2pF	6k	2V/83MHz	32	39.29	32.67	6.23	5.13	5.17
1MHz	1.8	4pF	2pF	6k	2V/83MHz	64	42.88	39.62	6.83	6.29	2.59
1MHz	1.8	4pF	2pF	6k	5V/100MHz	32	37.84	30.47	5.99	4.77	6.25
1MHz	1.8	4pF	2pF	6k	5V/100MHz	64	41.30	40.66	6.57	6.46	3.13
1MHz	2	4pF	2pF	6k	2V/83MHz	32	41.02	33.17	6.52	5.21	5.17
1MHz	2	4pF	2pF	6k	2V/83MHz	64	46.48	44.00	7.42	7.01	2.59

Similar to our first order table, we can note that changing the sampling frequency is what mainly affects our SNR, with a lower sampling frequency being more optimal for our design to prioritize higher SNR.

<u>Improvements made and alternatives</u>:

Comparator

The initial comparator used is seen below:

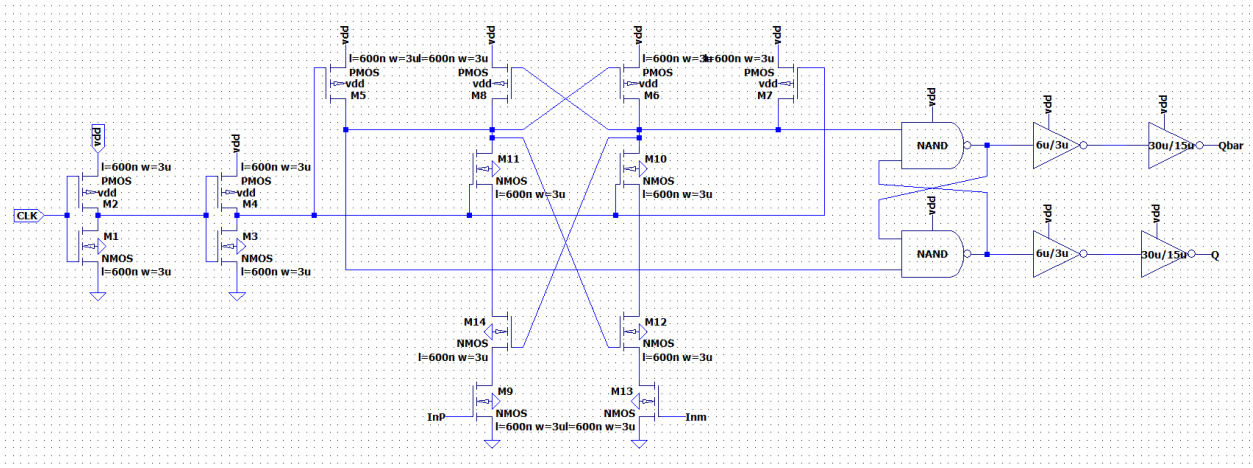


Figure 28. Initial comparator design

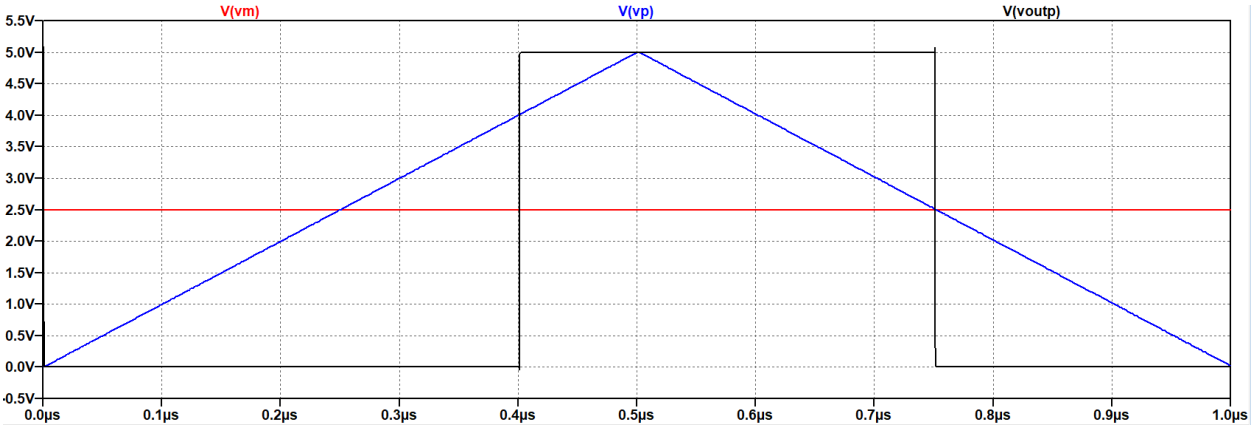


Figure 29. Initial comparator simulation

We can note the delayed response of the comparator on the rising edge, by about 150ns. This delayed response time prompted a different design to be tested and tried. While changing some widths of some transistors could easily change how fast this comparator makes a decision (which was used in the final design anyway), an alternative comparator was considered and tested, shown below.

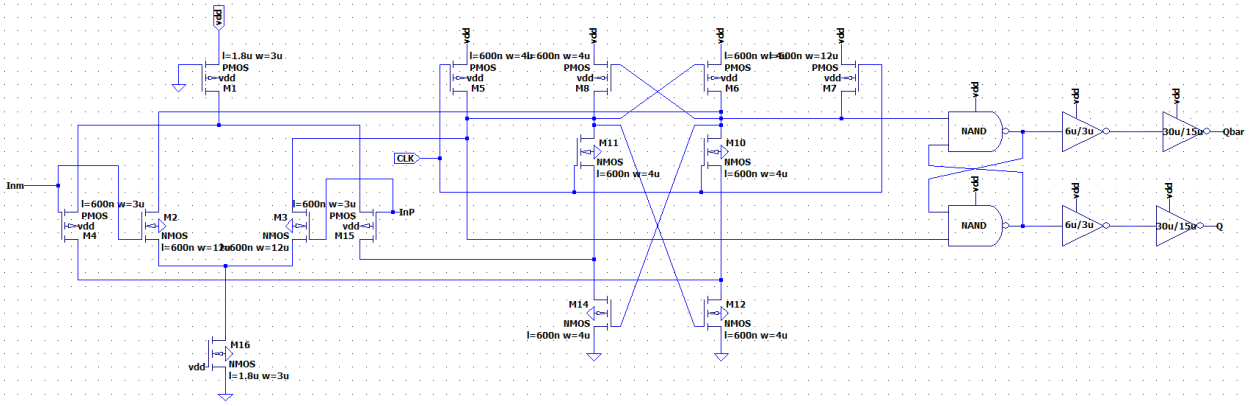


Figure 30. Alternative comparator that was considered

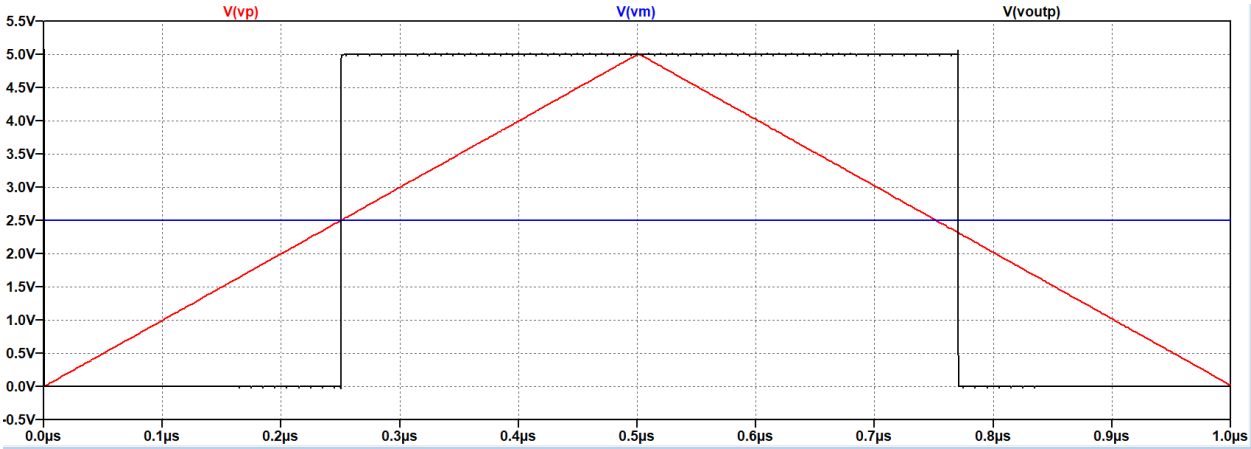


Figure 31. Alternative comparator simulation

We can note the evident change within our response time. This comparator is shown to make a decision pretty instantaneously and has added benefits to this topology such better sensitivity, a wider input signal swing, and an even bigger reduction in kickback noise. The cost of these advantages, however, would likely be that it would consume more power due to the long L MOSFETs required to drive the biasing of the circuit as well as more MOSFETs needed for the overall design. This instantaneous decision making of the comparator was also ultimately designed using the initial comparator (as previously mentioned and used in the overall design). Both has fast decision making and was tested in the 4-path 2nd order KD1S topology, but with the overall design used, it seemed like there were no drastic changes in terms of performance when simulation waveforms and SNR were compared for both comparator schematics, so the previous basic design was chosen due to the potential savings in power consumption. A better design for this alternative comparator could have potentially improved the SNR, but this design opted for the simpler, initial design.

Conclusion

In summary, this report compared an 8-Path 1st order KD1S modulator with a 4-Path 2nd order KD1S modulator within a continuous-time topology. The goal of this paper was to evaluate and compare the performance of both these modulators to analyze its SNR, effective number of bits, power consumption, and overall waveform results. This paper also discussed each component used and how they integrated their individual performance towards the overall performance of the topologies designed, as well as individual simulation results for each major component used.

Hand calculations were performed to determine a baseline for what we should be expecting, given that our components were ideal. However, the differences shown between the hand calculations and simulation results showed us that non-idealities introduced in real life models can greatly affect the actual values of our SNR and number of effective bits. The simulations also showed us how robust our overall designs were to changes in input frequency, sampling frequency, and amplitude with both topologies being tested at different parameters.

The data gathered in this paper showed that the second order topology was better than the first order topology in multiple ways such as better SNR and less dead zones, at the cost of more power being dissipated. However, if less power is required for a particular system, the first order design can be used since it still shows a reasonable SNR, just not as high as the second order topology. A direct comparison of the table results is seen below for convenience.

8-Path 1st Order KD1S Performance:

Input Frequency = 1MHz						
OSR	**64**		**128**		**256**	
Mode	**Serial**	**Parallel**	**Serial**	**Parallel**	**Serial**	**Parallel**
Fs new(MHz)	663	83	663	83	663	83
SNR (dB)	36.81	25.22	40.27	33.99	44.99	41.11
Neff (bits)	5.82	3.89	6.39	5.35	7.18	6.53
Bandwidth (MHz)	5.18		2.59		1.29	
Power Consumption	44.5mW					

4-Path 2nd Order KD1S Performance:

Input Frequency = 1MHz						
OSR	**32**		**64**		**128**	
Mode	**Serial**	**Parallel**	**Serial**	**Parallel**	**Serial**	**Parallel**
Fs new(MHz)	331	83	331	83	331	83
SNR (dB)	39.40	34.41	42.55	40.92	45.69	45.44
Neff (bits)	6.25	5.42	6.77	6.50	7.29	7.25
Bandwidth (MHz)	5.17		2.58		1.29	
Power Consumption	70.4mW					

In terms of future works and improvements, a possible component to consider improving our comparator, such as the alternative one mentioned earlier in the paper, to have faster design times at lower power. The clock generator could also be optimized to produce closer to 50% duty cycles to reduce jitter with perfect alignments between the complementary phi signals. The amplifier used in this design was simple, worked at high speeds, but cost us our gain, so designing an amplifier that has higher gain (or consumes less power) would also better optimize our overall performance.